WHAT IS CLAIMED IS:

1. A method for dynamic buffer allocation of shared memory within a multiple function integrated circuit, the method comprises:

determining mode of operation of the multiple function integrated circuit;

identifying at least one active module of a plurality of modules of the multiple function integrated circuit requiring a buffer based on the mode of operation;

determining buffer requirements for the at least one active module; and

allocating memory space of the shared memory for the buffer to be used by the at least one active module.

2. The method of Claim 1, wherein the at least one active module comprises at least two of:

a processing unit;

universal serial bus (USB) device;

digital to analog converter (DAC); and

analog to digital converter (ADC).

3. The method of Claim 1, wherein the mode of operation comprises at least one mode of operation selected from the group comprising:

a digital audio player mode;

a file storage device mode;

a digital multimedia player mode;

an extended memory device mode;

a digital audio recorder mode;

a digital multimedia recorder mode; and

a personal data assistant.

4. The method of Claim 1, further comprises:

changing the mode of operation of the multiple function integrated circuit to a second mode of operation;

identifying at least one other active module of the plurality of modules requiring another buffer based on the second mode of operation;

determining buffer requirements for the at least one other active module; and

allocating memory space of the shared memory for the another buffer to be used by the at least one active module.

5. The method of Claim 1, wherein the at least one active module has digital memory access (DMA) to the shared memory.

6. The method of Claim 5, wherein the shared memory comprises on-chip random access memory.

7. A method for dynamic buffer allocation of shared memory within a multiple function integrated circuit during initialization of the multiple function integrated circuit, the method comprises:

determining a first mode of operation of the multiple function integrated circuit;

identifying at least one active module of a plurality of modules of the multiple function integrated circuit requiring a buffer based on the first mode of operation;

determining buffer requirements for the at least one active module; and

allocating memory space of the shared memory for a buffer to be used by the at least one active module.

8. The method of Claim 7 that further comprises:

detecting activation of the multiple function integrated circuit;

9. The method of Claim 8 that further comprises:

detecting a change from the first mode of operation of the multiple function integrated circuit to a second mode of operation;

identifying at least one active module of the plurality of modules of the multiple function integrated circuit requiring a buffer based on the second mode of operation;

determining buffer requirements for the at least one active module; and

allocating memory space of the shared memory for a buffer to be used by the at least one active module.

10. The method of Claim 8, wherein the at least one active module comprises:

a processing unit;

universal serial bus (USB) device;

digital to analog converter (DAC); and

analog to digital converter (ADC).

11. The method of Claim 8, wherein the first mode of operation and second mode of operation comprise at least one mode of operation selected from:

a digital audio player mode;

a file storage device mode;

a digital multimedia player mode;

an extended memory device mode;

a digital audio recorder mode;

a digital multimedia recorder mode; and

a personal data assistant.

12. The method of Claim 8, wherein the at least one active module has digital memory access (DMA) to the shared memory.

13. The method of Claim 11, wherein the shared memory comprises on-chip random access memory.

14. An apparatus for dynamic buffer allocation of shared memory within a multiple function integrated circuit, the apparatus comprises:

processing module; and

memory operably coupled to the processing module, wherein at least portion of the memory functions as the shared memory and wherein the memory stores operational instructions that cause the processing module to:

detect activation of the multiple function integrated circuit;

determine a first mode of operation of the multiple function integrated circuit;

identify the at least one active modules of the multiple function integrated circuit requiring a buffer based on the first mode of operation;

determine buffer requirements for the at least one identified active module; and

allocate memory space within the RAM for a buffer to be used by the at least one active module.

15. The apparatus of Claim 14 wherein the memory further stores operational instructions that cause the processing module to:

detect a change from the first mode of operation of the multiple function integrated circuit to a second mode of operation;

identify at least one active module of the plurality of modules of the multiple function integrated circuit requiring a buffer based on the second mode of operation;

determine buffer requirements for the at least one active module; and

allocate memory space of the shared memory for a buffer to be used by the at least one active module.

16. The multiple function integrated circuit of Claim 13, wherein the at least one active module further comprises at least one of:

universal serial bus (USB) device;

a flash memory device;

an electronically programmable read only memory (EPROM) device;

a multi-wire device;

a hard drive device;

digital to analog converter (DAC); and

analog to digital converter (ADC).

17. The multiple function integrated circuit of Claim 13, wherein the first mode of operation and second mode of operation comprise at least one mode of operation selected from:

a digital audio player mode;

a file storage device mode;

a digital multimedia player mode;

an extended memory device mode;

a digital audio recorder mode;

a digital multimedia recorder mode; and

a personal data assistant.

18. The multiple function integrated circuit of Claim 13, wherein the at least one active module has digital memory access (DMA) to the shared memory.

19. The multiple function integrated circuit of Claim 13, wherein the processing module determines the first mode of operation from initialization inputs to the multiple function integrated circuit, wherein the initialization inputs identify active modules operable coupled to the multiple function integrated circuit.

20. The multiple function integrated circuit of Claim 18, wherein the active modules include at least one of:

universal serial bus (USB) device;

a flash memory device;

an electronically programmable read only memory (EPROM) device;

a multi-wire device;

a hard drive device;

digital to analog converter (DAC); and

analog to digital converter (ADC).